REMARKS

This application has been carefully reviewed in light of the final office action mailed July 17, 2002. Claims 1-25 are pending in this application. Applicants respectfully request early and favorable acceptance of this application.

Rejections under 35 U.S.C. § 103

Claims 1-25 are rejected under 35 U.S.C. § 103(a) as being anticipated by Madson et al. (U.S. Patent Application Number US2001/0049167) in combination with Williams et al. (U.S. Patent 6,291,298). Applicants respectfully traverse the rejection.

Claim 1 recites a method of forming a trench in a semiconductor device, comprising, among other things, forming a protruding portion (e.g., 18) in a masking material (e.g., 14), depositing a semiconductor material (e.g., 24), removing the protruding portion to form the trench, and etching the semiconductor material to round off corners (e.g., 28) of the trench.

The Madson reference discloses several methods of manufacturing a trench transistor in which a semiconductor material is deposited in a region defined by a dielectric pillar. A portion of the dielectric pillar is etched, leaving a dielectric plug of predetermined thickness, and the trench is formed over the dielectric plug.

The Williams reference discloses a method of forming a trench device wherein the trench is formed with rounded corners in an epi layer (i.e., 220) by isotropic and anisotropic plasma etching.

The Madson reference does not show or teach the step of removing a protruding portion of a masking material to form a trench or of etching the trench to round off corners of the trench. All of the Madson devices are shown having a dielectric plug terminating on the top of the dielectric plug in the trench as described in paragraphs [0028], [0036], [0044], [0058], [0062] and [0070]. The dielectric plug allows the Madson devices to achieve a high breakdown voltage and low or predetermined drain to gate capacitance (paragraphs 59,62 and 70).

M.P.E.P. § 706.02(j) indicates that any teaching or suggestion to make the claimed combination must be found in the prior art references. There is no teaching, suggestion or motivation contained in the Madson reference for combining the Madson and Williams et al. references. In order to round the corners of the Madson trench, the oxide pillar would have to removed or else voids would form along the sides of the pillar. However, the Madson reference teaches away from a rounding etch by disclosing the trench etch terminating on the top of the oxide pillars (¶¶ [0007], [0028], [0044]). Moreover, there would be no motivation to combine the Madson and Williams et al. references because the Madson devices use the oxide pillar remaining in the trench to obtain a high breakdown voltage and low, and/or predetermined, drain to gate capacitance. Since the objectives of the Madson device are achieved by leaving the oxide pillar in the trench, there would be no motivation to add processing steps to remove the oxide pillar from the trench because such a step would effectively defeat one of the purpose of the Madson device. More processing steps would then be needed to incorporate the Williams et al. etch step to round off corners of the trench to provide the high breakdown voltage that was already present

with the oxide pillar.

Finally, even if the Madson device were combined with the Williams et al. device and voids were not produced along the sides of the dielectric plug, the result would be a device having a plug of oxide left from the pillar in the bottom of the trench, and would not have the advantage taught by the applicant of improved depth control, breakdown improvements and accurate alignment of the trench bottom to the foundation layer (e.g., 12) as described in the specification on page 7, line 15 through page 9, line 24. Furthermore, such a device would not have the rounded off semiconductor material on top of a foundation layer 12 as does the applicant. Instead, the rounding would occur on top of the Madson plug resulting in poor channel resistance.

Thus, the combination of the Madson and Williams references do not show or teach a method of forming a trench in a semiconductor device, comprising, among other things, forming a protruding portion in a masking material, depositing a semiconductor material, removing the protruding portion to form the trench, and etching the semiconductor material to round off corners of the trench as does the applicant.

Therefore, Applicants believe claim 1 is not anticipated by the Madson reference in view of the Williams reference. Claims 2-8 depend from an allowable base claim and therefore are allowable for at least the same reasons.

For reasons similar to those stated regarding claim 1, Applicants believe that independent claims 9 and 17, which include the steps of removing a protruding portion to form the trench, are not anticipated by the reference. Claims 10-16 depend from claim 9, which is believed allowable, and therefore are allowable as well. Claims 18-25 depend from

base claim 17, and are therefore believed allowable.

CONCLUSION

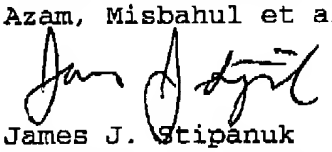
Applicants have made an earnest attempt to place this case in condition for allowance. In light of the above remarks, applicants respectfully request reconsideration and allowance of claims 1-25.

Applicants have reviewed the other prior art made of record and believe that such art does not affect the patentability of the claimed invention.

No fees are believed due pursuant to rule 1.136(a), but the Commissioner is hereby authorized to charge any fees or credit any overpayment to Deposit Account 501086.

If there are matters which can be discussed by telephone to further the prosecution of this application, applicants invite the examiner to call the undersigned attorney at the examiner's convenience.

Respectfully submitted,
Azam, Misbahul et al., by



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